AMENDMENTS TO THE CLAIMS:

1. (Currently amended) A microcomputer, comprising:

a central processing unit;

a data bus electrically connected to said central processing unit;

a cache;

a command bus electrically connected to said cache and said central processing unit and separated from said data bus; and

a first memory electrically connected to said command bus, said first memory storing an interruption handling routine therein,

said cache being electrically connected to a second memory.

2. (Original) The microcomputer as set forth in claim 1, wherein a program is written into said memory by switching memory maps when said microcomputer is turned on.

3. (Previously presented) The microcomputer as set forth in claim 1, wherein said memory comprises a command random access memory.

4. (Currently Amended) A microcomputer, comprising:

first, second, third, and fourth buses, the second bus being separated from the first bus;

a central processing unit;

a bus controller electrically connected to said central processing unit through said first bus;

a command cache electrically connected to said central processing unit through said second bus and to said bus controller through said third bus; and

a command memory electrically connected to said second bus through said fourth bus, ~~for~~ said command memory storing an interruption handling routine therein.

5. (Previously presented) The microcomputer as set forth in claim 4, further comprising fifth, sixth, and seventh buses; and a memory controller electrically connected to said bus controller through said fifth bus and to said command memory through said sixth bus, and adapted to be connected to an external memory through said seventh bus.

6. (Previously presented) The microcomputer as set forth in claim 5, wherein, when said memory controller is connected to the external memory through said seventh bus, said central processing unit is responsive to said command cache storing a command to be executed by said central processing unit, to read said command out of said command cache and to execute the thus read-out command, and said central processing unit is further responsive to said command cache not storing a command to be executed by said central processing unit, to read a command out of the external memory and to execute the thus read-out command.

7. (Previously presented) The microcomputer as set forth in claim 4, wherein said central processing unit is responsive to an interruption, to read a command out of said command memory and to execute the interruption handling routine.

8. (Currently Amended) A ~~The~~ microcomputer, ~~as set forth in claim 4, further~~ comprising:

first, second, third, and fourth buses;

a central processing unit;

a bus controller electrically connected to said central processing unit through said first bus;

a command cache electrically connected to said central processing unit through said second bus and to said bus controller through said third bus;

a command memory electrically connected to said second bus through said fourth bus, for storing an interruption handling routine therein; and

an external terminal electrically connected to said central processing unit, and wherein a region in which said command memory is to be arranged is designated through said external terminal.

9. (Previously presented) The microcomputer as set forth in claim 8, wherein said external terminal can be operated while said central processing unit is in operation.

10. (Currently Amended) A ~~The~~ microcomputer, ~~as set forth in claim 4, further~~ comprising:

first, second, third, and fourth buses;

a central processing unit;

a bus controller electrically connected to said central processing unit through said first bus;

a command cache electrically connected to said central processing unit through said second bus and to said bus controller through said third bus;

a command memory electrically connected to said second bus through said fourth bus, for storing an interruption handling routine therein; and

an external terminal electrically connected to said central processing unit, and wherein memory maps are switched through said external terminal.

11. (Original) The microcomputer as set forth in claim 4, further comprising an internal register, and wherein memory maps are switched by said internal register.

12. (Previously presented) The microcomputer as set forth in claim 4, wherein said memory comprises a random access memory.

13. (Previously presented) The microcomputer as set forth in claim 1, wherein said cache comprises a command cache.

14. (Previously presented) The microcomputer as set forth in claim 1, further comprising a further bus adapted to be connected to an external memory storing a program to be executed by said microcomputer.

15. (Currently Amended) A ~~The~~ microcomputer, ~~as set forth in claim 1, further~~ comprising:

a central processing unit;

a data bus electrically connected to said central processing unit;

a cache;

a command bus electrically connected to said cache and said central processing unit and separated from said data bus;

a memory electrically connected to said command bus and electrically isolated from said data bus, said memory storing an interruption handling routine therein; and

an external terminal electrically connected to said central processing unit, and wherein a region in which said memory is to be arranged is designated through said external terminal.

16. (Previously presented) The microcomputer as set forth in claim 15, wherein said external terminal can be operated while said central processing unit is in operation.

17. (Currently Amended) A ~~The~~ microcomputer, ~~as set forth in claim 1, further~~ comprising:

a central processing unit;

a data bus electrically connected to said central processing unit;

a cache;

a command bus electrically connected to said cache and said central processing unit and separated from said data bus;

a memory electrically connected to said command bus and electrically isolated from said data bus, said memory storing an interruption handling routine therein; and

an external terminal electrically connected to said central processing unit, and wherein memory maps are switched through said external terminal.

18. (Previously presented) The microcomputer as set forth in claim 1, wherein said central processing unit is responsive to an interruption, to read a command out of said memory and to execute the interruption handling routine.